

Preliminary Amendment

Applicant: Josef Böck et al.

Serial No.: Unknown

(Priority Application No. DE 102 31 407.1)

(International Application No. PCT/EP2003/007553)

Filed: Herewith

(Priority Date July 11, 2002)

(International Filing Date July 11, 2003)

Docket No. I435.121.101/12307

Title: BIPOLAR TRANSISTOR

REMARKS

This Preliminary Amendment amends the above-identified Utility Patent Application filed herewith. With this Preliminary Amendment, claims 1-8 have been cancelled. Claims 9-32 have been added. Claims 9-32 remain pending in the application and are presented for consideration and allowance.

A substitute specification is included herewith. The specification contains no new matter.

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CONCLUSION

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 500471.

Any inquiry regarding this Preliminary Amendment should be directed to Steven E. Dicke at the below-listed telephone numbers.

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The Examiner is invited to contact the Applicants' representative at the below-listed telephone number to facilitate prosecution of this application.

Respectfully submitted,

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I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313.1450.

By Vanessa Carels
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Description

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BIPOLAR TRANSISTOR**Field of the Invention**

This invention concerns a bipolar transistor which can be, in particular, in the form of a ~~so-called~~ self-aligned bipolar transistor.

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Background

In the case of bipolar transistors, the ~~so-called~~ extrinsic base resistance, with the transition frequency and base collector capacitance, is one of the decisive transistor parameters which determine important characteristic quantities such as the maximum oscillation frequency, the amplification ("gain"), the minimum noise factor, gate delay times, etc. of the bipolar transistor. The extrinsic base resistance corresponds to the resistance between the base, or the actual base area, and an external contact, which is connected to the base via a connecting line.

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Regarding the above-mentioned transistor parameters, the following applies, for instance, to the maximum oscillation frequency f_{\max} of the bipolar transistor:

25

$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi \cdot R_B \cdot C_{BC}}} \quad \dots(1)$$

where f_T is the transition frequency, R_B is the extrinsic base resistance and C_{BC} is the base collector capacitance of the bipolar transistor.

30

For the minimum noise factor F_{\min} of a bipolar transistor, the following applies, depending on the extrinsic base resistance R_B and frequency f :

$$F_{\min} \approx 1 + \frac{1}{\beta} + \frac{f}{F_T} \cdot \sqrt{\frac{2 \cdot I_C}{V_T} \cdot R_B \cdot \left(1 + \frac{f_T^2}{\beta \cdot f^2}\right)} + \frac{f_T^2}{\beta \cdot f^2} \quad \dots(2)$$

where β is the small signal current amplification, I_C is the collector current, and V_T is the thermal voltage of the bipolar transistor.

From the two formulae (1) and (2), it can be seen that the extrinsic base resistance R_B should be small for fast switching and low noise factors. One method of reducing losses in the case of bipolar transistors is the use of a polysilicon electrode for contacting the base. A p^+ polysilicon layer provides a low-resistance path with correspondingly low capacitance for the base current.

Specially small extrinsic base resistances can be achieved, for instance, by use of the concept of the so-called "self-aligned double polysilicon bipolar transistor", as described in "Self-Aligned Bipolar Transistors for High-Performance and Low-Power-Delay VLSI", T.H. Ning et al., IEEE Transactions on Electron Devices, Vol. ED-28, No. 9, pp. 1010 - 1013, 1981. This concept is therefore used in almost all widely used production technologies for ultra-high frequency bipolar transistors.

Summary

The present invention provides a bipolar transistor. Embodiments of the invention provide a bipolar transistor and method of making a bipolar transistor. In one embodiment, the invention provides a bipolar transistor having a polysilicon layer into which impurity atoms are inserted, thereby reducing the layer resistance.

In the attached figure 1, such a self-aligned npn double polysilicon bipolar transistor is shown in cross-section. The emitter 3 is contacted via an n+ doped polysilicon electrode 1. A p+ polysilicon electrode 2 is assigned to the p+ doped base 4. The self-aligned emitter base insulation 7 is called the "spacers". Additionally, under the emitter electrode 3 a TEOS ("tetraethoxysilan / tetraethylorthosilicate") insulation layer 6 is provided, and under the base electrode 2 a LOCOS ("local oxidation of silicon") insulation layer 8 is provided. In the figure, the collector area 5 of the bipolar transistor (without the associated collector electrode) is also shown by a dashed line. A method of producing such a bipolar transistor is described, for instance, in EP-B1-0 535 350.

In the case of a self-aligned double polysilicon bipolar transistor such as is shown in the figure, the extrinsic base resistance R_B consists essentially of three parts, which are called below the "internal" resistance part R_{Bi} , the "external" resistance part R_{Be} , and the "link" resistance part R_{Bl} . The internal resistance part R_{Bi} results from the resistance in the base area 4 on the active transistor area. The external resistance part R_{Be} describes the resistance of the polysilicon base electrode 2, which leads to the external base contact. The link resistance part R_{Bl} represents the extrinsic base resistance which results from the low-doped zone under the self-aligned emitter base insulation, the spacers 7.

In today's bipolar transistors, the total extrinsic base resistance R_B is usually dominated by the sum of the internal resistance part R_{Bi} and the link resistance part R_{Bl} . Because of progressing lateral scaling of the components, the internal resistance part R_{Bi} and the link resistance part R_{Bl} are continually being reduced. Simultaneously, the external resistance part R_{Be} is constantly increasing, because the vertical component scaling which is linked to the lateral scaling requires ever thinner polysilicon layers as connecting electrodes, and the layer resistance of these connecting areas is thus constantly increasing. Thus the external resistance part R_{Be} is becoming ever more important for the total extrinsic base resistance R_B .

To keep the layer resistance of the base electrode 2 as small as possible, in general polysilicon layers doped with boron are used. The boron doping is chosen to be above the electrically activatable concentration of typically greater than $5 \times 10^{20} \text{ cm}^{-3}$, to achieve the smallest possible layer resistance. The boron doping atom is chosen because of the consideration that boron has little or no effect on the grain growth, and does not tend to separate at the grain boundaries during thermal processing events. The model of doping material separation assumes that the conductivity is controlled by separation of doping atoms at the grain boundaries, where the atoms are themselves captured and become electrically inactive. Additionally, a high doping material concentration at the grain boundaries suppresses grain growth during annealing. Redistribution of implanted doping materials and greater grain sizes during subsequent annealing steps change the electrical and structural properties of the layers, which clearly affects the external resistance part R_{Be} of the extrinsic base resistance R_B . The main problem is the annealing behaviour of Si samples with doping atoms. In fact, only a small proportion of the doping atoms, about 10%, is ionised. It is assumed that inactive, non-eliminated doping atoms are present in cluster form. Cluster formation of the doping atoms takes place at the annealing temperature, or alternatively mainly during cooling of the sample. With typical doping values of boron greater than $5 \times 10^{20} \text{ cm}^{-3}$ and a layer thickness of 150 - 250 nm, minimum layer resistances of about 50 - 100 Ω/\square can be achieved.

~~The present invention is based on the object of providing a bipolar transistor in which the layer resistance of the connecting electrodes, particularly the base electrode, is further reduced.~~

~~This object is achieved according to the invention by a bipolar transistor with the features of Claim 1. In the subclaims, preferred and advantageous embodiments of this invention are given.~~

According to the invention, it is proposed that in bipolar transistors, instead of traditional polysilicon electrodes, polysilicon layers into which impurity atoms are inserted should be used. These cause a high density of vacancies in the electrode material.

5

As impurity atoms, preferably C, P or Ar atoms are used, C atoms being specially preferred. The density of the impurity atoms in the polysilicon layer is preferably in the range of about 10^{19} — 10^{21} cm⁻³.

- 10 Carbon with high solubility in silicon can be built into the silicon lattice at the interstices and also at the more favourable (in energy terms) lattice sites, in exchange for a Si atom. The C atoms at the lattice sites capture Si atoms which are present at interstices, and thus form bound interstitial complexes. Because of this capturing mechanism of the C atoms, additional vacancies are generated.
- 15 The carbon in the polysilicon layer therefore provides sinks for interstices during annealing, so that interstice driven cluster formation of, for instance, boron doping atoms is suppressed, and thus the quantity and concentration of active doping atoms can be increased. This results in a lower layer resistance of the polysilicon layer which is doped with, for instance, boron, and thus to a smaller
- 20 extrinsic base resistance. This effect can be further increased by the use of polysilicon layers of polycrystalline silicon-germanium.

- Since carbon is in general use in semiconductor technology, and can be inserted into the polysilicon layer of the electrodes both directly during layer
- 25 growth and by ion implantation, the concept of the invention, as described above, can be implemented simply and economically in manufacturing methods for traditional bipolar transistors.

- A further advantage is that C atoms can be built in without essentially
- 30 interfering with the Si lattice structure, since the volume of even SiC is only about 3% greater than that of pure Si.

Although this invention refers in particular to bipolar transistors, in principle use with other transistor types such as FET, MOS or CMOS transistors is also conceivable.

5

Brief Description of the Drawings

The invention is explained in more detail below, referring to the only figure of a preferred embodiment.

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~~Regarding the embodiment which is shown in the figure, to avoid repetition reference can be made to a large extent to the above explanation of the prior art. As mentioned above, in the figure a self-aligned npn bipolar transistor is shown in cross-section. Fig. 1 is a cross-section illustrating one exemplary embodiment of a bipolar transistor according to the invention.~~

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Detailed Description

The present invention provides a bipolar transistor in which the layer resistance of the connecting electrodes, particularly the base electrode, is further reduced.

According to one embodiment of the invention, it is proposed that in bipolar transistors, instead of traditional polysilicon electrodes, polysilicon layers into which impurity atoms are inserted should be used. These cause a high density of vacancies in the electrode material.

As impurity atoms, preferably C, P or Ar atoms are used, C atoms being specially preferred. The density of the impurity atoms in the polysilicon layer is preferably in the range of about $10^{19} - 10^{21} \text{ cm}^{-3}$.

Carbon with high solubility in silicon can be built into the silicon lattice at the interstices and also at the more favourable (in energy terms) lattice sites, in exchange for a Si atom. The C atoms at the lattice sites capture Si atoms which are present at interstices, and thus form bound interstitial complexes. Because of

this capturing mechanism of the C atoms, additional vacancies are generated. The carbon in the polysilicon layer therefore provides sinks for interstices during annealing, so that interstice-driven cluster formation of, for instance, boron doping atoms is suppressed, and thus the quantity and concentration of active
5 doping atoms can be increased. This results in a lower layer resistance of the polysilicon layer which is doped with, for instance, boron, and thus to a smaller extrinsic base resistance. This effect can be further increased by the use of polysilicon layers of polycrystalline silicon-germanium.

Since carbon is in general use in semiconductor technology, and can be
10 inserted into the polysilicon layer of the electrodes both directly during layer growth and by ion implantation, the concept of the invention, as described above, can be implemented simply and economically in manufacturing methods for traditional bipolar transistors.

A further advantage is that C atoms can be built in without essentially
15 interfering with the Si lattice structure, since the volume of even SiC is only about 3% greater than that of pure Si.

Although this invention refers in particular to bipolar transistors, in principle use with other transistor types such as FET, MOS or CMOS transistors is also conceivable.

20 The emitter 3 of the bipolar transistor is contacted via an n+ doped polysilicon electrode 1, and a p+ polysilicon electrode 2 is assigned to the p+ doped base 4. Spacers 7 are provided as the self-aligned emitter base insulation. Additionally, under the emitter electrode 1 a TEOS insulation layer 6 is provided, and under the base electrode 2 a LOCOS insulation layer 8 is
25 provided. In the figure 1, the collector area 5 of the bipolar transistor is also ~~shown~~illustrated by a dashed line.

As the base electrode 2, a polysilicon layer, into which C impurity atoms are inserted with a concentration of $10^{19} - 10^{21} \text{ cm}^{-3}$, is used. This can be
30 done either by ion implantation or alternatively directly during layer growth, without an additional implantation step. Additionally, as already known, the

polysilicon layer is doped with boron atoms at a concentration of greater than $5 \times 10^{20} \text{ cm}^{-3}$.

5 The C impurity atoms incorporate themselves into the Si lattice at
interstices and preferably at the more favourable (in energy terms) lattice sites.
The C impurity atoms on the lattice sites capture Si atoms from interstices and
form bound interstitial complexes. Because of these captured Si atoms,
additional vacancies are formed, with an estimated density of about 10^{19} cm^{-3} .
The Si-C agglomerates which are formed in this way are stable to about 700°C .
10 At higher temperatures, they are converted to $\beta \text{ SiC}$. The volume of SiC, which
is greater by about 3% compared with the Si matrix, can also easily be
compensated for by vacancies, so that no undesired voltages occur in the
electrodes. In this way, during annealing, the carbon generates sinks for
interstices in the polysilicon layer, so that interstice-driven cluster formation of
15 the boron doping atoms is suppressed and thus the quantity of active doping
atoms can be increased.

 The higher concentration of active doping atoms which is generated in
this way results in a lower layer resistance of the polysilicon layer, which is
20 doped with boron, and thus to a smaller extrinsic base resistance. This effect
can be further increased by the use of polysilicon layers of polycrystalline
silicon-germanium.

 Obviously, alternatively or additionally to the base electrode 2, the
25 emitter electrode 1 and the collector electrode can be in the form according to
the invention.